Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	701	438/296.ccls. and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2006/02/02 09:48
L2	5	1 and (substrate with (carbide or (gallium adj nitride)))	US-PGPUB; USPAT	OR	ON	2006/02/02 08:23
L3	8234	((nitride or hafnium or scandium) with trench) and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2006/02/02 09:22
L4	5371	3 and (trench with isolation)	US-PGPUB; USPAT	OR	ON	2006/02/02 09:22
L5	3210	4 and CMP	US-PGPUB; USPAT	OR	ON	2006/02/02 09:22
L6	653	((nitride or hafnium or scandium) with trench with liner) and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2006/02/02 09:22
L7	561	6 and (trench with isolation)	US-PGPUB; USPAT	OR	ON	2006/02/02 09:22
L8	386	7 and CMP	US-PGPUB; USPAT	OR	ON	2006/02/02 09:46
L9	4646	(polysilicon with lpcvd)	US-PGPUB; USPAT	OR	ON	2006/02/02 09:47
L10	3627	(polysilicon with lpcvd) and temperature	US-PGPUB; USPAT	OR	ON	2006/02/02 09:48
L11	3407	10 and semiconductor	US-PGPUB; USPAT	OR	ON	2006/02/02 09:48
L12	3072	11 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2006/02/02 09:48

US-PAT-NO: 6894357

DOCUMENT-IDENTIFIER: US 6894357 B2

TITLE: Gate stack for high performance sub-micron CMOS devices

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Detailed Description Text - DETX (25):
Specifically, the layer 52 of gate dielectric is to comprise a layer of material having a high dielectric constant. As examples of dielectric materials with high dielectric constant can be cited SiN (7.4) and Al.sub.3 O.sub.3 (8.5). Other materials that meet requirements of high dielectric constant are titanium oxide (TiO.sub.2), zirconium oxide (ZrO.sub.2), tantalum oxide (Ta.sub.2 O.sub.5), barium titanium oxide (BaTiO.sub.3) and strontium titanium oxide (SrTiO.sub.3) This layer 52 is preferably deposited to a thickness between about 25 and 200 Angstrom and more preferably to a thickness of about 50 Angstrom, using methods of LPCVD procedures at a pressure between about 200 mTorr and 800 mTorr, at a **temperature** between about 500 and 700 degrees C., followed by annealing at a **temperature** between about 700 and 900 degrees C.

Detailed Description Text - DETX (26):
The bottom gate electrode layer 54 preferably comprises **polysilicon**-germanium or doped **polysilicon,** layer 54 is deposited using **LPCVD** procedures, at a **temperature** between about 500 and 700 degrees C., to a thickness between about 500 to 5000 Angstrom. Layer 54 of doped polysilicon be in-situ doped with an impurity implant of phosphorous (n-type impurity) or boron (p-type impurity).

Detailed Description Text - DETX (30):
The layer 56 of top gate material preferably comprises undoped **polysilicon,** deposited using **LPCVD** procedures, at a **temperature** between about 600 and 800 degrees C., to a thickness between about 500 to 5000 Angstrom.

Detailed Description Text - DETX (35):
The layer 58, FIG. 3, of silicon nitride (Si.sub.3 Ni.sub.4) can be deposited using LPCVD or PECVD procedures at a pressure between about 200 mTorr and 400 mTorr, at a **temperature** between about 600 and 800 degrees C., to a thickness of about 100 and 400 Angstrom using NH.sub.3 and SiH.sub.4 or

SiCl.sub.2 H.sub.2. The silicon nitride layer 58 can also be deposited using LPCVD or PECVD procedures using a reactant gas mixture such as dichlorosilane (SiCl.sub.2 H.sub.2) as a silicon source material and ammonia (NH.sub.3) as a nitrogen source, at a **temperature** between about 600 and 800 degrees C., at a pressure between about 300 mTorr and 400 mTorr, to a thickness between about 100 and 400 Angstrom.

Detailed Description Text - DETX (40):

Typical processing conditions for the formation of layer 60 of TiN are as follows: source: titanium nitride, at a **temperature** of about 25 to 150 degrees C., a pressure of about 100 to 150 mTorr, for a time duration of about 5 to 10 seconds, using Ar as sputtering ions.

Detailed Description Text - DETX (43):

Layer 60, if this layer is selected to comprise TiN, can be etched using anisotropic etching with an etchant gas of one of the group of CF.sub.4, CHF.sub.3, CHCl.sub.3, CCl.sub.4, BCl.sub.4 and Cl.sub.2 at a **temperature** between about 100 and 200 degrees C.

Detailed Description Text - DETX (44):

Layer 58, if this layer is selected to comprise silicon nitride, can be etched with a silicon nitride etch recipe comprising CHF.sub.3 at a flow rate between about 0 and 100 sccm, CF.sub.4 at between about 0 and 50 sccm and Ar at a flow rate between about 50 and 150 sccm. Silicon nitride layer 58 can also be etched using a SiON or SiN removal process with etchant gasses CH.sub.3 F/Ar/O.sub.2 at a **temperature** between about 10 and 20 degrees C., a pressure of between about 50 and 60 mTorr with an etch time of between about 40 and 60 seconds. The silicon nitride layer 58 can also be wet etched using a buffered oxide etchant (BOE). The BOE may comprise a mixed solution of fluoroammonium and fluorohydrogen (7:1) and phosphoric acid solution. The silicon nitride layer 58 can also be etched using anisotropic RIE using CHF.sub.3 or SF.sub.6 --O.sub.2 or SF.sub.6 /HB.sub.8 as an etchant. The preferred method of removing silicon nitride is an isotropic wet etch process using hot phosphoric acid. The silicon nitride layer 58 can also be dipped into phosphoric acid (H.sub.3 PO.sub.4) to be removed. The nitride layer can also be removed from the trenches created in the layer of photoresist by dipping the structure into hot phosphoric acid (H.sub.3 PO.sub.4) (standard wet nitride removal).

Detailed Description Text - DETX (46):

The removal of patterned layer 62 of photoresist is performed applying conventional methods of photoresist removal, as previously highlighted. Patterned layer 60, FIG. 4, can be etched using anisotropic etching with an

etchant gas of one of the group of CF.sub.4, CHF.sub.3, CHCl.sub.3, CCl.sub.4, BCl.sub.4 and Cl.sub.2 at a **temperature** between about 100 and 200 degrees C. As an alternative method, layer 60 may be removed applying methods of Chemical Mechanical Polishing, down to the surface of layer 58 of hard mask material such as silicon nitride. For polishing of the layer 60, the hard mask layer 58 forms a good interface for end-point detection of the polishing step.

Detailed Description Text - DETX (63):

After the source/drain regions 65/67 have been implanted into the surface of substrate 10, the structure will be subjected to RTA to activate source/drain implanted species and may be subjected to a step of vacuum baking in order to further solidify the surface of the second gate spacers 70. This vacuum bake is in-situ or ex-situ vacuum baking the substrate at a **temperature** in the range of about 300 to 350 degrees C. for a time between about 25 and 35 minutes and a pressure between about 0.5 and 1000 mTorr.

Detailed Description Text - DETX (67):

To reduce contact resistance with the points of electrical contact of the gate electrode, these contact regions are salicided. This is accomplished by forming a silicide film of a metal that has a high melting point on these surfaces. A titanium silicide film is mainly used as the high melting point silicide film while cobalt silicide and nickel silicide film have also been investigated. The basic success of forming salicided contact layers can be achieved due to the fact that certain metals, such as titanium or cobalt, react when heated while they are in contact with silicon or doped or undoped polysilicon. This reaction forms conductive silicides over the surface of these layers while the metal however does not react with silicon oxides. By forming silicon oxide spacers on the sidewalls of the gate electrode, the deposited metal does not interact with the sidewalls of the gate electrode and separate points of electrical contact can be formed for the source/drain regions and the surface of the gate electrode. The salicided source contact surface has been highlighted with surface region 76, FIG. 12, the salicided drain contact surface has been highlighted with surface region 78, the salicided gate electrode contact surface has been highlighted with surface region 74. The process of salicidation can be applied using two thermal anneals, a first anneal to convert the deposited layer of metal to a salicided material, the second anneal to convert the salicided material to a low resistivity phase. The anneal to form thin layers of salicided material, such as titanium silicide (TiSi.sub.2) over the source/drain regions and the gate structure can therefore be a rapid first thermal anneal in a **temperature** range of between 600 and 700 degrees C. for a time of between 20 and 40 seconds, followed by a rapid second thermal anneal in a **temperature** of between about 800

and 900 degrees C. for a time between 20 and 40 seconds. As for cobalt silicide, the first annealing is a RTA at a **temperature** in the range of 480 to 520 degrees C., followed by a second RTA at a **temperature** in the range of 800 and 850 degrees C.